REMARKS

The Examiner has removed previous objections to the Specification and Claims and previous rejections to the Claims except rejections to all pending Claims as either anticipated by U.S. Patent No. 5,717,359 issued to Matsui or obvious over Matsui taken alone or in combination with U.S. Patent No. 6,061,222 issued to Morris. Applicants respectfully traverse and request reconsideration of the Examiner's rejections for full allowance of all pending claims.

1. Claim Rejections Under Section 102.

Claims 1 and 10 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,717,359 issued to Matsui et al.

Matsui discloses a semiconductor integrated circuit with terminal pad connections that include a pad for a power source and a ground. Matsui discloses the use of a bypass capacitor disposed between the power source and ground to reduce noise. (1:48-51). Matusi further discloses routing a source line and ground line from the power source and ground to an integrated circuit to increase the parasitic inductance of the power and ground lines to reduce noise.

Claim 1 recites, in part, "a series-resonant impedance coupled to the first pad, the series-resonant impedance comprising a serpentine conductor deposited on the circuit board and a tuning capacitance deposited on the circuit board."

Claim 10 as amended recites, in part, "means coupled to the capacitor for attenuating signals at F_o, the means comprising a serpentine conductor and a tuning capacitance, the serpentine conductor and tuning capacitance deposited on the printed circuit board."

Matsui cannot anticipate Claims 1 or 10 because Matsui fails to teach, disclose or suggest all elements recited by Claims 1 and 10. For instance, Matsui fails to teach, disclose or suggest a "a series resonant impedance comprising a serpentine conductor deposited on the circuit board and a tuning capacitance deposited on the circuit board" as recited by Claim 1. Matsui fails to teach, disclose or suggest a "means comprising a serpentine conductor and tuning capacitance

deposited on the printed circuit board" as recited by Claim 10. Instead, Matusi uses routing of power and ground lines to increase parasitic inductance. The power and ground lines of Matsui are routed to an integrated circuit, not a tuning capacitor. The Examiner's position that Figure 5 of Matsui discloses a LC circuit based on the inherent capacitance of the routed line of Matusi has no support. Applicants respectfully submit that the capacitance of Figure 5 is provided by a bypass capacitor, also recited in Claims 1 and 10, and not a tuning capacitor which Matsui fails to disclose. Accordingly, Applicants respectfully request that the Examiner withdraw the rejections of Claims 1 and 10 and the rejections to Claims 2-9, 11-19 and 21, which depend from Claims 1 and 10 respectively.

2. *Rejections under Section 103.*

Claim 22 stands rejected under 35 U.S.C. § 103 as being unpatentable over Matsui. Claims 29 and 36 stand rejected under 35 U.S.C. § 103 as being unpatentable over Matsui in view of U.S. Patent No. 6,061,222 issued to Morris et al.

Morris discloses an integrated circuit structure.

Claim 22 recites, in part, "attaching a discrete capacitor to a printed circuit board (PCB) between a power pad and a reference pad; depositing an inductance on the PCB so that the inductance is connected at a first end to the power pad; forming a tuning capacitance on the PCB so that the tuning capacitance is connected to a second end of the inductance."

Claim 29 recites, in part, "a terminating segment coupling a second linear segment to the capacitive element."

Claim 36 recites, in part, "means, including an inductance and a capacitance, coupled to the first pad for suppressing spurious signals at a predetermined frequency, the capacitance formed by a conductor deposited on a surface of the printed circuit board and separated from the ground plane by the printed circuit board to have a predetermined tuning capacitance set by the printed circuit board dielectric thickness."

Matsui and Morris, considered either separately or in combination, cannot make obvious Claims 22, 29 or 36 because Matsui and Morris fail to teach, disclose or suggest all elements

recited by Claims 22, 29 or 36. As described above, Matsui fails to teach, disclose or suggest both a bypass capacitance between a power and ground pad and also an inductance and tuning capacitance interfaced with the power pad. Morris fails to disclose the elements missing from Matusi. Accordingly, Matsui and Morris cannot make obvious Claim 22, 29 and 36, and Applicants respectfully request that the Examiner withdraw the rejection of Claims 23-28, 30-35 and Claims 36-39, which depend respectively from Claims 22, 29 and 36.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being transmitted via facsimile to: COMMISSIONER FOR PATENTS, Washington, D.C. 20231, on March 17, 2003.

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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